L Number	Hits	Search Text	DB	Time stamp
4	2584	undoped with (silicon silicate) with oxide usg	USPAT; EPO; JPO	2004/03/19 10:31
5	12740	phosphosilicate with glass psg	USPAT; EPO; JPO	2004/03/19 10:32
6	16603	sion (silicon silicate) with oxynitride	USPAT; EPO; JPO	2004/03/19 10:33
7	199	(undoped with (silicon silicate) with oxide usg) and (phosphosilicate with glass psg) and (sion (silicon silicate) with oxynitride)	USPAT; EPO; JPO	2004/03/19 10:33
9	9	((undoped with (silicon silicate) with oxide usg) and (phosphosilicate with glass psg) and (sion (silicon silicate) with oxynitride)) and integrated adj circuit and active with (area region) and plug$4 and metal adj layer	USPAT; EPO; JPO	2004/03/19 14:57
10	1	6492224.pn.	USPAT; EPO; JPO	2004/03/19 11:03
11	1	6144060.pn.	USPAT; EPO; JPO	2004/03/19 11:03
15	1	((undoped with (silicon silicate) with oxide usg) and (phosphosilicate with glass psg) and (sion (silicon silicate) with oxynitride)) and integrated adj circuit and active with (area region) and solder$4 and etch$3 and polyimide and metal adj layer	USPAT; EPO; JPO	2004/03/19 15:50
16	2	("5220199" | "6037668").PN.	USPAT	2004/03/19 15:28
17	9	6232662.URPN.	USPAT	2004/03/19 15:29
35	1	((undoped with (silicon silicate) with oxide usg) and (phosphosilicate with glass psg) and (sion (silicon silicate) with oxynitride)) and integrated near3 circuit and active with (area region) and solder$4 and etch$3 and polyimide and metal adj layer	USPAT; EPO; JPO	2004/03/19 15:50
36	1	((undoped with (silicon silicate) with oxide usg) and (phosphosilicate with glass psg) and (sion (silicon silicate) with oxynitride)) and active with (area region) and solder$4 and etch$3 and polyimide and metal adj layer	USPAT; EPO; JPO	2004/03/19 15:51
37	8	((undoped with (silicon silicate) with oxide usg) and (phosphosilicate with glass psg) and (sion (silicon silicate) with oxynitride)) and active with (area region) and (connect connecting connection) and etch$3 and polyimide and metal adj layer	USPAT; EPO; JPO	2004/03/19 17:11
40	3	((undoped with (silicon silicate) with oxide usg) and (phosphosilicate with glass psg) and (sion (silicon silicate) with oxynitride)) and redistribution	USPAT; EPO; JPO	2004/03/19 17:13
41	4	((undoped with (silicon silicate) with oxide usg) and (phosphosilicate with glass psg) and (sion (silicon silicate) with oxynitride)) and solder adj (ball bump)	USPAT; EPO; JPO	2004/03/19 17:16
42	0	((undoped with (silicon silicate) with oxide usg) and (phosphosilicate with glass psg) and (sion (silicon silicate) with oxynitride)) and 29/$.ccls.	USPAT; EPO; JPO	2004/03/19 17:17
43	158	((undoped with (silicon silicate) with oxide usg) and (phosphosilicate with glass psg) and (sion (silicon silicate) with oxynitride)) and 257/$.ccls.	USPAT; EPO; JPO	2004/03/19 17:17

44	8	(((undoped with (silicon silicate) with oxide usg) and (phosphosilicate with glass psg) and (sion (silicon silicate) with oxynitride)) and 257/$.ccls.) and metal adj pad	USPAT; EPO; JPO	2004/03/19 17:18
-	1	redistribution.ti. and danielle.in.	USPAT; US-PGPUB; EPO; JPO	2004/03/18 17:16
-	17	redistribution adj layer and plug	USPAT; EPO; JPO	2004/03/18 18:04
-	3774	active with circuit with area	USPAT; EPO; JPO	2004/03/18 17:20
-	2362	(active with circuit with area) and integrated adj circuit	USPAT; EPO; JPO	2004/03/18 17:21
-	577	((active with circuit with area) and integrated adj circuit) and metal adj layer	USPAT; EPO; JPO	2004/03/18 17:21
-	405	(((active with circuit with area) and integrated adj circuit) and metal adj layer) and connect$3 and etch$3	USPAT; EPO; JPO	2004/03/18 17:22
-	235	((((active with circuit with area) and integrated adj circuit) and metal adj layer) and connect$3 and etch$3) and silicon with oxide	USPAT; EPO; JPO	2004/03/18 17:29
-	19	(((((active with circuit with area) and integrated adj circuit) and metal adj layer) and connect$3 and etch$3) and silicon with oxide) and glass adj layer and substrate	USPAT; EPO; JPO	2004/03/18 17:39
-	0	(active with circuit with area) and glass adj layer and undoped with silicon and polyimide and etch$3 and connect$3 and metal adj layer	USPAT; EPO; JPO	2004/03/18 17:41
-	22	(active with circuit with area) and glass with layer and oxide with silicon and polyimide and etch$3 and connect$3 and metal adj layer	USPAT; EPO; JPO	2004/03/18 17:42
-	3	redistribution adj layer and (active with circuit with area)	USPAT; EPO; JPO	2004/03/18 18:05
-	9	redistribution with (film layer) and (active with circuit with area)	USPAT; EPO; JPO	2004/03/18 18:14
-	1632	undoped with silicon with oxide	USPAT; EPO; JPO	2004/03/18 18:40
-	4223	phosphosilicate with glass	USPAT; EPO; JPO	2004/03/18 18:41
-	7474	silicon with oxynitride	USPAT; EPO; JPO	2004/03/18 18:41
-	76	(undoped with silicon with oxide) and (phosphosilicate with glass) and (silicon with oxynitride)	USPAT; EPO; JPO	2004/03/18 18:16
-	30	((undoped with silicon with oxide) and (phosphosilicate with glass) and (silicon with oxynitride)) and plug$3	USPAT; EPO; JPO	2004/03/18 18:17
-	30	((undoped with silicon with oxide) and (phosphosilicate with glass) and (silicon with oxynitride)) and plug$4	USPAT; EPO; JPO	2004/03/18 18:19
-	55	((undoped with silicon with oxide) and (phosphosilicate with glass) and (silicon with oxynitride)) and (ic chip integrated adj circuit)	USPAT; EPO; JPO	2004/03/18 18:20
-	2541	(undoped with silicon with oxide) usg	USPAT; EPO; JPO	2004/03/18 18:40
-	13084	(phosphosilicate with glass) bpsg	USPAT; EPO; JPO	2004/03/18 18:41
-	16545	(silicon with oxynitride) sion	USPAT; EPO; JPO	2004/03/18 18:41
-	6	((undoped with silicon with oxide) usg) and ((phosphosilicate with glass) bpsg) and ((silicon with oxynitride) sion) and integrated adj circuit and active with circuit with (area region) and plug$4	USPAT; EPO; JPO	2004/03/18 18:43

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	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current
30	☐	☑	US 6483150 B1	20021119	11	Semiconductor device with both memories and logic	257/368	257/E21. 257/E21.
31	☐	☑	US 6426556 B1	20020730	16	Reliable metal bumps on top of I/O pads with test probe	257/738	257/762
32	☐	☑	US 6291307 B1	20010918	13	Method and structure to make planar analog capacitor on	438/393	257/E21. 257/E21.
33	☐	☑	US 6274899 B1	20010814	13	Capacitor electrode having conductive regions adjacent	257/298	257/301; 257/303;
34	☐	☑	US 6197641 B1	20010306	17	Process for fabricating vertical transistors	438/268	257/E21. 257/E29.
35	☐	☑	US 6117766 A	20000912	10	Method of forming contact plugs in a semiconductor	438/637	257/E21. 257/E21.
36	☐	☑	US 6100202 A	20000808	15	Pre deposition stabilization method for forming a void	438/734	257/E21. 257/E23.
37	☐	☑	US 6037220 A	20000314	13	Method of increasing the surface area of a DRAM	438/255	257/E21. 257/E21.
38	☐	☑	US 6027975 A	20000222	15	Process for fabricating vertical transistors	438/268	257/E21. 257/E29.
39	☐	☑	US 6576941 B1	20030610	15	Ferroelectric capacitors on protruding portions of	257/295	257/306
40	☐	☑	US 6238968 B1	20010529	17	Methods of forming integrated circuit	438/253	257/E21. 438/254;
41	☐	☑	US 6232662 B1	20010515	10	System and method for bonding over active	257/750	257/734; 257/E23.
42	☐	☑	US 6380087 B1	20020430	12	CMP process utilizing dummy plugs in damascene process	438/692	438/622; 438/627;
43	☐	☑	US 5766974 A	19980616	7	Method of making a dielectric structure for	438/624	257/E21. 257/E21.
44	☐	☑	US 4990464 A	19910205	4	Method of forming improved encapsulation layer	117/43	117/904; 148/DIG.

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